IN THE CLAIMS

1. (Currently amended) A flash memory device comprising:

a memory cell array block having a plurality of flash memory cells arrayed therein;

a program verification voltage generator structured to variably generate program verification voltages to verify whether the flash memory cells are programmed or not; and

a word line level selector structured to transfer the program verification voltages to word lines connected to control gates of the flash memory cells[[.]] ;

wherein the program verification voltage generator comprises:

a PMOS transistor and a series of resistors, which are connected between a power supply voltage and a ground reference voltage;

a first NMOS transistor connected to both terminals of a first resistor and structured to electrically short the first resistor in response to a first program verification control signal and to generate a program verification voltage at a node between drains of the PMOS transistor and the first NMOS transistor;

a second NMOS transistor connected to both terminals of a second resistor and structured to electrically short the second resistor in response to a second program verification control signal; and

a comparator structured to compare a reference voltage to a voltage of a node between the first and second resistors, and having an output connected to a gate of the PMOS transistor.

2. (Cancelled)

3. (Currently Amended) The flash memory device of claim 1 ~~claim 2~~, wherein the first and second program verification control signals are selectively activated to change levels of the program verification voltages.

4. (Original) The flash memory device of claim 1, wherein the word line level selector is structured to apply a programming voltage, a read voltage, a pass voltage, or an erase voltage to the word lines of the flash memory cells according to operation modes.

5. (Previously presented) In a flash memory device including one or more flash memory cells, a method of verifying whether the flash memory cells are programmed or not, the method comprising:

repeating a program unit loop cycle of:

applying predetermined programming voltages to the flash memory cells,

variably generating program verification voltages, and

verifying whether the flash memory cells are programmed or not in response to the program verification voltages;

until the programming of the flash memory cells is completed, wherein the program verification voltages are changed between two or more program unit loop cycles.

6. (Original) The method of claim 5, wherein the program verification voltage at an nth program unit loop cycle has a higher voltage level than the program verification voltage at an (n-1)th program unit loop cycle.

7. (Original) The method of claim 6, wherein the program verification voltage at an (n+1)th program unit loop cycle has a lower voltage level than the program verification voltage at the nth program unit loop cycle.

8. (Original) The method of claim 7, wherein the program verification voltage at the (n-1)th program unit loop cycle has the same level as the program verification voltage at the (n+1)th program unit loop cycle.

9. (Original) The method of claim 5, wherein the program verification voltages at the (n-1)th, nth and (n+1)th program unit loop cycles have different voltage levels from each other.

10. (Original) The method of claim 5, wherein the program verification voltage at an nth program unit loop cycle has a lower voltage level than the program verification voltage at an (n-1)th program unit loop cycle, and the program verification voltage at an (n+1)th program unit loop cycle has a lower voltage level than the program verification voltage at the nth program unit loop cycle.

11. (Currently amended) A programming unit for a non-volatile memory device, comprising:

[[an]] a first input structured to accept a programming verification control signal;

a second input structured to accept a second programming verification control signal;

a voltage generator structured to generate at an output a programming verification voltage having a voltage level selected from more than [[one]] two possible ~~level~~ levels, the voltage level of the programming verification voltage dependent on a state of the programming verification control ~~signal~~ signals; and

a word line transfer unit coupled to the output of the voltage generator and structured to transfer the programming verification voltage to one or more word lines in the memory device.

12. (Cancelled)

13. (Currently amended) The programming unit of ~~claim 12~~ claim 11 wherein the first input is coupled to a control gate of a transistor and wherein the second input is coupled to a control gate of a second transistor.

14. (Currently amended) The programming unit of ~~claim 12~~ claim 11 wherein the voltage generator comprises:

a serial transistor coupled to a voltage supply;

a first and second resistor coupled in series between the serial transistor and a ground reference voltage;

a first control transistor coupled across the first resistor and structured to cause a short across the first resistor when controlled by the programming verification control signal; and

a second control transistor coupled across the second resistor and structured to cause a short across the second resistor when controlled by the second programming verification control signal.

15. (Original) The programming unit of claim 14, further comprising:

a comparator structured to compare a voltage of a node between the first and second transistors to a reference voltage.

16. (Original) The programming unit of claim 15 wherein an output of the comparator is coupled to a control input of the serial transistor.

17. (New) A flash memory device comprising:

a memory cell array block having a plurality of flash memory cells arranged in word lines and bit lines; and

a program verification voltage generator structured to generate a program verification voltage to be supplied to a selected word line every program loop;

wherein the program verification voltage generator is structured to generate the program verification voltage at an nth program unit loop cycle so as to be higher or lower than that for a (n-1)th program unit loop cycle.

18. (New) The flash memory device of claim 17, further comprising a word line level selector structured to transfer the program verification voltage to the selected word line connected to control gates of the flash memory cells.

19. (New) The flash memory device of the claim 17, wherein the program verification voltage at the nth program unit loop cycle ha a higher voltage level than the program verification voltage at the (n-1)th program unit loop cycle.

20. (New) The flash memory device of claim 19, wherein the program verification voltage at an (n+1)th program unit loop cycle has lower voltage level than the program verification voltage at the nth program unit loop cycle.

21. (New) the flash memory device of claim 20, wherein the program verification voltage at the (n-1)th program unit loop cycle has the same level as the program verification voltage at the (n+1)th program unit loop cycle.

22. (New) The flash memory device of claim 21, wherein the program verification voltage at the (n-1)th, nth and (n+1)th program unit loop cycles have different voltage levels from each other.

23. (New) The flash memory device of claim 17, wherein the program verification voltage at the nth program unit loop cycle has a lower voltage level than the program verification voltage at the (n-1)th program unit loop cycle, and the program verification voltage at an (n+1)th program unit loop cycle has a lower voltage level than the program verification voltage at the nth program unit loop cycle.

24. (New) The flash memory device of claim 17, wherein the program verification voltage comprises:

a PMOS transistor and series of resistors, which are connected between a power supply voltage and a ground reference voltage;

a first NMOS transistor connected to both terminals of a first resistor and structured to electrically short the first resistor in response to a first program verification control signal and to generate a program verification voltage at a node between drains of the PMOS transistor and the first NMOS transistor;

a second NMOS transistor connected to both terminals of a second resistor and structured to electrically short the second resistor in response to a second program verification control signal; and

a comparator structured to compare a reference voltage to a voltage of a node between the first and second resistors, and having an output connected to a gate of the PMOS transistor.

25. (New) The flash memory device of claim 24, wherein the first and second program verification control signals are selectively activated to change levels of the program verification voltage.

26. (New) The flash memory device of claim 18, wherein the word line level selector is structured to apply a programming voltage, a read voltage, a pass voltage, or an erase voltage to the word lines of the flash memory cells according to operation modes.